What is claimed is:

1. An ashing method comprising:

an in situ baking step, wherein a silicon substrate is baked for a predetermined period of time under a pressure of 10 Torr or more while said silicon substrate is placed on a hot plate;

a vacuumizing step, wherein a stable vacuum status is achieved while said silicon substrate is placed on said hot plate;

a gas processing step, wherein selected reaction gas is introduced into a reaction chamber; and

an ashing step, wherein plasma is generated until almost all of the photoresists are removed.

2. The ashing method as set forth in Claim 1, wherein the temperature of said hot plate is from 200° C through 300° C.

3. The ashing method as set forth in Claim 2, wherein the temperature of said hot plate is from 230° C through 270° C

4. The ashing method as set forth in Claim 1, wherein said predetermined period of time at said in situ baking step is longer than five seconds, but not longer than twenty seconds.

5. The ashing method as set forth in Claim 1, wherein said reaction gas comprises one or more of O_2, N_2, H_2N_2, O_3, or CF_4.

6. The ashing method as set forth in Claim 1, wherein said silicon substrate is dose ion implanted.

7. The ashing method as set forth in Claim 1, wherein said silicon substrate is a via-etched substrate.

8. The ashing method as set forth in Claim 1, wherein said silicon substrate is a pad-etched substrate.

9. The ashing method as set forth in Claim 1, comprising additionally an over-ashing step, in which plasma is continuously generated even after almost all of the photoresists have been removed by plasma generated at said ashing step.